

2708/2716 EPROM BOARD

INSTRUCTION MANUAL

ISSUED SEPT. 1977

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TABLE OF CONTENTS

Circuit features.....1
Assembly instructions.....2
Address selection chart.....4
Debug instructions.....5
Circuit description.....6
Parts list.....7
Schematic.....8

REVISION

The following jumpers are required ONLY when using Intel 2716's, and should NOT be installed for operation with 2708's.

Jumper +5 volts from the output of Q₁ (the rightmost pin, when viewed from the component side, of the bottom regulator) to the rightmost pin (again from the component side) of:

1. Q₂ (-5V regulator) and
2. Q₄ (-5V regulator)

Note that Q₂ and Q₄ are not installed when using 2716's.

CIRCUIT FEATURES

- Accepts up to 16 of either 2708 or 2716 EPROMS or compatible ROMS.
- Board addressable to any 16k boundary: EPROM'S addressable by DIP switch to any 1k (2k with 2716) location.
- Only those EPROMS installed need be enabled. Unused locations may be allocated for RAM.
- Selectable wait states.
- All S-100 lines fully buffered.

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2. Q₄ (-5v regulator)

Note that Q₂ and Q₄ are not installed when using 2716's.

ASSEMBLY INSTRUCTIONS

- 1) Install IC sockets at all locations EXCEPT SW1 and SW2.
- 2) Install DIP switches at locations SW1 and SW2.
- 3) Install $.1\mu\text{F}$ capacitors at locations C4-C8, C13-C19, C28 and C29-C52.
- 4) Install $.22\mu\text{F}$ capacitors at locations C1, C3, C9, C11, C25, C27, C53 and C55.
- 5) Install $47\mu\text{F}$ capacitors at locations C2, C10, C26 and C54. Note that all the capacitors are installed with "+" to the right.
- 6) Install the 5V regulator (7805) at Q1.
- 7) Install the -5V regulator (7905) at Q2 and Q4. Make sure to install a mica washer between the tab and the heatsink, THIS IS IMPORTANT!
- 8) Install the 12V regulator (7812) at Q3.
- 9) Install the two $4.7\text{k}\Omega$ SIPS.
- 10) Install the appropriate jumper at J9 and J10 to select either 2708 or 2716 EPROMS. J9 is for the upper row, J10 for the lower.



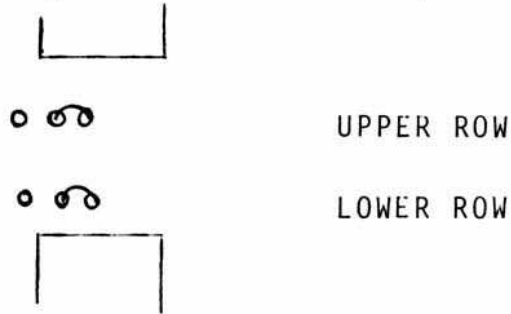
JUMPERING FOR 2708



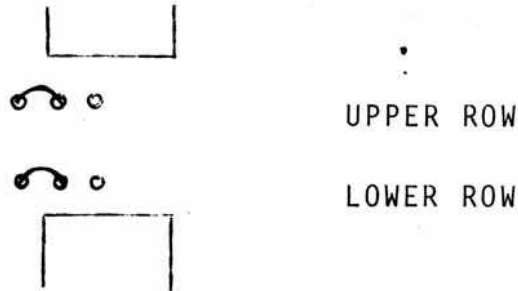
JUMPER FOR 2716

- 11) Install the appropriate jumpers at J1 through J8 to select 2708's or 2716's. Make sure this conforms with the jumpering at J9 and J10.

J1
 (J2 through J8 are identical)



SELECTS 2708'S ON BOTH UPPER
 AND LOWER ROW.



SELECTS 2716'S ON BOTH UPPER
 AND LOWER ROW.

One row can be set for 2708's while the other is set for 2716's. But 2708's and 2716's may not be mixed within a row. We note again that jumpers J1 through J8 must conform with J9 and J10; i.e. you must be consistent.

12) Jumper the board for the required number of wait states:

(J12)	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
	No wait states	1 wait state	2 wait state	3 wait state	4 wait state

<u>Processor</u>	<u>Speed</u>	<u>Chip</u>	<u>Access time</u>	<u>No. of wait state</u>
8080 or Z-80 or similar	2MHz	2708 or 2716	450nS	0
8080 or Z-80 or similar	2MHz	2708S	650nS	1
Z-80A	4MHz	2708 or 2716	450nS	1
Z-80A	4MHz	2708S	650nS	2

13) Set the Bank address. When using 2708's the board is configured for one of the four possible 16k blocks, while with 2716's choose the lower or upper 32K.

<u>16K Page</u>	<u>Block</u>	Using 2708's (J11)	
		<u>Hex Address</u>	<u>Jumper Setting</u>
1	0-16K	0000-3FFF	0 0 0 0 0 0 0 0
2	16K-32K	4000-7FFF	0 0 0 0 0 0 0 0
3	32K-48K	8000-BFFF	0 0 0 0 0 0 0 0
4	48K-64K	C000-FFFF	0 0 0 0 0 0 0 0

Using 2716's			
1	0-32K	0-7FFF	0 0 0 0 0 0 0 0
2	32K-64K	8000-FFFF	0 0 0 0 0 0 0 0

14) DIP SWITCH SELECTION:

In any bank, the topmost switch addresses the right most EPROM. The lowest switch addresses the left most EPROM.

DEBUG INSTRUCTIONS

- 1) Check the board visually for cold solder joints, shorts and unsoldered pins.
- 2) Check the polarities on all electrolytic capacitors.
- 3) Power the board up and check all the voltages at the regulators, and then at the EPROM sockets.

<u>VOLTAGE</u>	<u>2708 Pin #</u>	<u>INTEL 2716 Pin #</u>
+5	24	24
-5	21	NC
+12v.	19	NC

- 4) Install the remaining IC's.
- 5) Using the front panel check the address lines A0 through A9 (A10 for the 2716) pins on the EPROMS. Do this by examining 0000H and check that all address lines are low, then examine 03FFH and check to see that they are all high. By trying a few more combinations, verify that there are no lines shorted together. Incorrect results are usually the result of either a line shorted to Ground, a line shorted to +5V, or two lines shorted together. The most common cause is a bad solder joint or solder bridge, so inspect the board closely. An ohm meter is a help here. If you can find no errors check out IC's 5, 6 and 7.
- 6) Check A10 through A15 by the method above but look at the appropriate pin of IC 14, 24 and 2. Check that the chip selects are being properly decoded by the 1 of 8 decoders, IC 14 and 24. Check the enable lines pin #4, 5, and 6. When the board is addressed they should be low, low and high respectively.
- 7) Lastly, check that chips 23 #8 and 13 #8 are gating the buffers on by looking for a low at IC 1-6 when you address an enabled 2708.
- 8) Insert a known 2708 and examine a few locations.

CIRCUIT DESCRIPTION

ADDRESS DECODING

The 2708/2716 Board requires only power, address lines A0-A15, SMEMR and PDBIN lines for proper operation. Optionally $\phi 2$, PSYNC and PRDY may be used to operate the wait state circuitry.

The 16 address lines are buffered by the non-inverting buffers IC's 5, 6 and 7. The least significant 10 address lines are connected directly to the 2708 EPROMS (11 in the case of 2716's), with the remaining 6 (5 for 2716's) decoded by the 1-of-8 decoders IC14 and IC24. These provide the individual chip selects. J9 and J10 select whether the decoders see address lines A10 through A13 or A11 through A14, and hence whether we decode 1K address spacing for the 2708 or 2k for the 2716.

The EPROM pins #19 see +12 volts (for the 2708) or A10 (for the 2716), depending on jumpers J1 through J8. This is the Intel 2716 standard. TI 2716's may be accommodated and an application note will be available for this shortly. The switches at locations SW1 and SW2 enable the EPROMS so that unused locations need not be allocated. IC's 13 and 23 enable the output buffers only for those locations which have been selected. IC1-8 is the EPROM ENABLED signal that indicates a valid location. It is AND'ED with SMEMR and PDBIN to generate the buffers enabled signal at IC1 pin 6.

WAIT STATE CIRCUITRY

At the beginning of each cycle PSYNC clears the register IC3. Successive $\phi 2$'s then clock the chip and shift highs into the register. Depending on the location of J12, PRDY is held low for 0, 1, 2 or 3 $\phi 2$ clock cycles. The valid EPROM signal at IC1-8 is anded with SMEMR at IC-12 to enable PRDY onto the bus.

PARTS LIST

U1	74LS10
U2	74LS04
U3	74LS173 (if no wait states; is unnecessary)
U4	Resister pac 4.7k
U5, U6, U7, U8	74LS367 or 8097 Or 8T97
U13, U23	74LS30
U14, U24	74LS138
U15, U22, U25-U32	2708 or 2716 (Intel recommended)*
Q1	7805 or LM740T-5.0
Q2, Q4	7905 or LM720T-5.0
Q3	7812 or LM740T-12

* Do Not Use TI

Caps

C4-C8, C12-C24, C28-C52 - 0.1 f ceramic	(43)
C2, 10 26, 54 - 47 uf 2 20vdc electrolytic	(4)
C1, C3, C9, C11, C25, C27, C53, C55, - 0.22 uf ceramic	(8)

Resistors

SIP 1,2 single in-line resistor pack 8-4.7k

Misc.

4 heat sinks for regulators
2 sets mounting hardware
2 sets nylon insulating screw, nut and washer
16-24 pin sockets
7-16 pin sockets
4-14 pin sockets

2708/2716 EPROM Board

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To make this manual more useful to you, our customer, we will appreciate your comments and recommendations on any improvements to this manual you feel are needed. After using this manual, please take the first opportunity to complete this questionnaire and return it, postpaid, to the factory where your comments will be given every consideration. Thank you.

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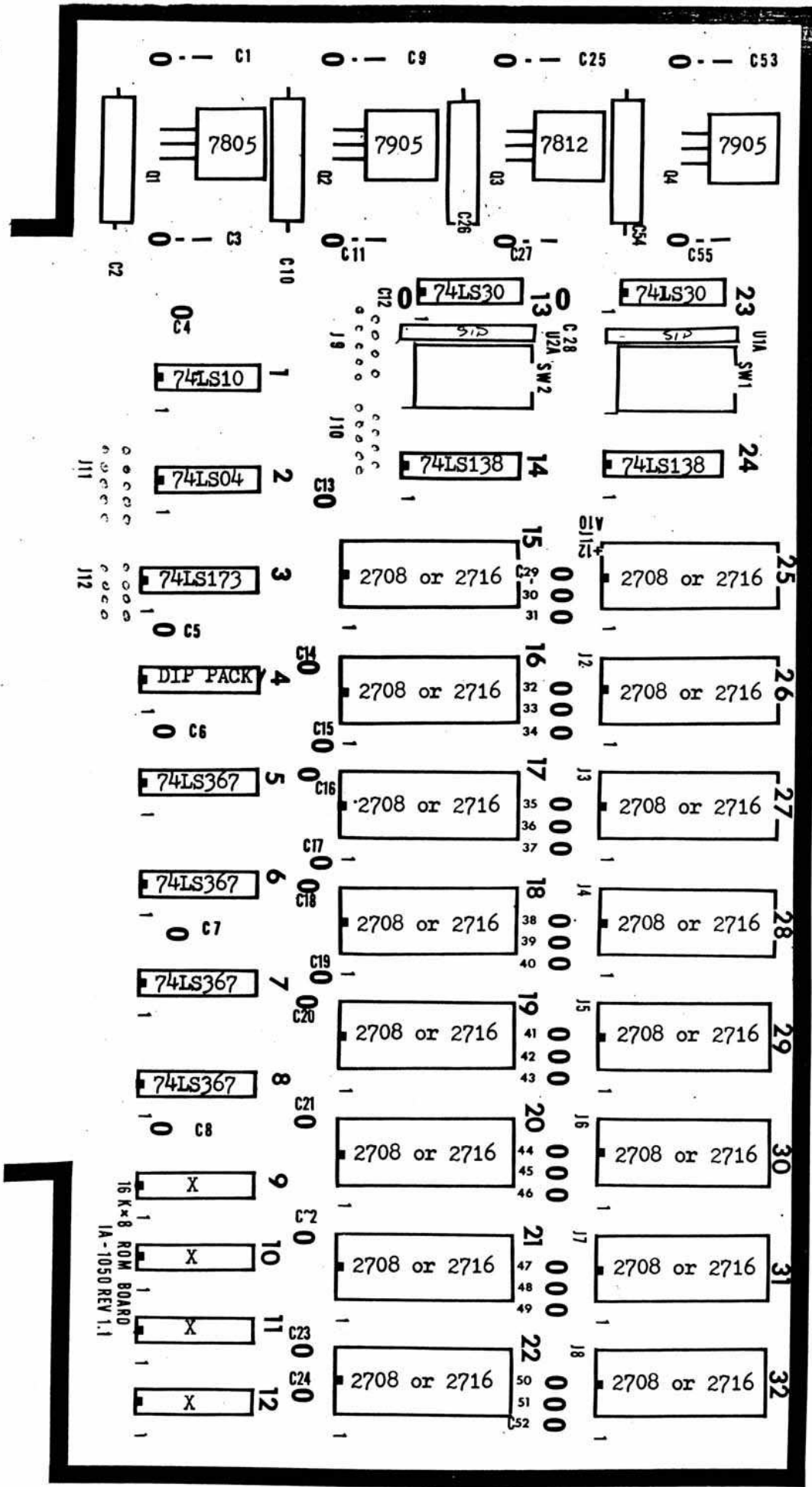
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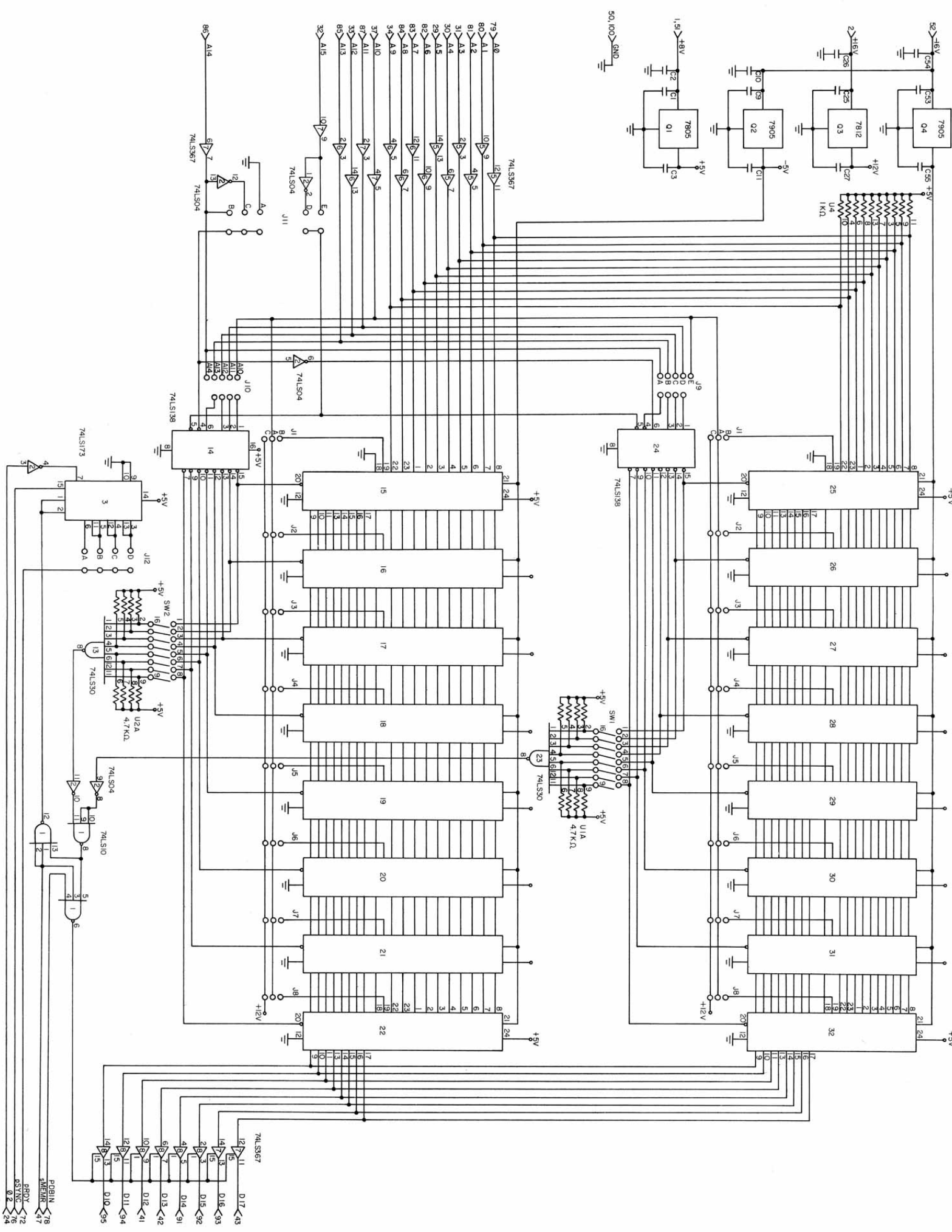
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POBIN 19
 PRRY 12
 637 NC 17
 16
 17
 24